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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,347	06/10/2005	Christophe Joly	PHUS020584	6792

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EXAMINER	
NGUYEN, HIEU P	
ART UNIT	PAPER NUMBER
2817	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,347	JOLY, CHRISTOPHE	
	Examiner	Art Unit	
	Hieu P. Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,7,8,11,13,14 and 17* is/are rejected.

7)☒ Claim(s) *3,4,6,9,10,12,15,16 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

Applicant is required to update the status (pending, allowed, etc.) of all parent priority applications in the first line of the specification. The status of all citations of US filed applications in the specification should also be updated where appropriate.

The specification has not been checked to the extent necessary to determine the presence to all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2, 7-8 and 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by **Taylor** (U.S. 6,233,440).

Regarding claim 1, Fig. 2 of Taylor discloses a radio frequency (RF) linear power amplifier operating in an output frequency band, having an output transistor (32), said power

amplifier comprising: (a) a circuit means (31) for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier (e.g. see col. 3, lines 44-47), (b) a detector circuit means (20/22) for detecting RF input to said amplifier and generating a driving signal (output signal from node 24) according to a power level of said RF input; (c) a self-adapting circuit means (26/28/30) for receiving said driving signal and automatically modifying said bias signal and said quiescent current through said output transistor as mentioned in col. 3, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels as broadly mentioned in col. 3 or mentioned in the abstract , **meeting claim 1**.

Regarding claim 7, similar to claim 1, Fig. 2 of Taylor discloses a device including a radio frequency (RF) linear power amplifier operating in an output frequency band, having an output transistor (32), said power amplifier comprising: (a) a circuit means (31) for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier (e.g. see col. 3, lines 44-47); (b) a detector circuit means (20/22) for detecting RF input to said amplifier and generating a driving signal (output signal from node 24) according to a power level of said RF input; (c) a self-adapting circuit means (26/28/30) for receiving said driving signal and automatically modifying said bias signal and said quiescent current through said output transistor as mentioned in col. 3, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels as mentioned in col. 3 or mentioned in the abstract, **meeting claim 7**.

Regarding claim 13, Taylor discloses in Fig. 2 a self-adapting circuit for dynamically controlling quiescent current flowing through said output transistor of a linear power amplifier

operating in an output frequency band, having an output transistor (32), said linear power amplifier comprising a circuit means (31) for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier (e.g. see col. 3, lines 44-47), said self-adapting bias circuit comprising: a) a detector circuit means (20/22) for detecting RF input to said amplifier and generating a driving signal (output current from node 24) according to a power level of said RF input; b) means (26/28/30) for receiving said driving signal and automatically modifying said bias signal and said quiescent current through said output transistor as mentioned in col. 3, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels as mentioned in col. 3 or mentioned in the abstract, **meeting claim 13**.

Regarding claims 2 and 8, Taylor discloses everything claimed as applied to claims 1 and 7. In addition, Taylor discloses in Fig. 2 the linear power amplifier as claimed in claim 1, wherein the self-adapting circuit means (26/28/30) automatically modifies said quiescent current for an output stage amplifier by tracking said detected RF signal being input to the amplifier at power ranges above a certain power output threshold (see Vref from numeral 27), **meeting claims 2 and 8**.

Regarding claim 14, Taylor discloses everything claimed as applied to claim 13. In addition, Taylor discloses in Fig. 2 the self-adapting circuit as claimed in claim 13, wherein the modifying means (26) automatically modifies said quiescent current for an output stage amplifier to track said detected RF signal being input to the amplifier at power ranges above a certain power output threshold (Vref from numeral 27), **meeting claim 14**.

Claims 1, 5, 7, 11, 13 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsumoto et al. (U.S. 6,710,649).

Regarding claim 1, Fig. 6 of Matsumoto discloses a radio frequency (RF) linear power amplifier operating in an output frequency band, having an output transistor (11), said power amplifier comprising: (a) a circuit means (3) for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier, (b) a detector circuit means (12) for detecting RF input to said amplifier and generating a driving signal (an output signal from collector terminal of the transistor 24) according to a power level of said RF input; (c) a self-adapting circuit means (e.g. 27/28) for receiving said driving signal (note: the driving signal is part of the current mirror as shown in Fig. 6, numerals 25/26) and automatically modifying said bias signal and said quiescent current through said output transistor as mentioned in col. 5, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels as mentioned in col. 2, **meeting claim 1**.

Regarding claim 7, similar to claim 1, Fig. 6 of Matsumoto discloses a device including a radio frequency (RF) linear power amplifier operating in an output frequency band, having an output transistor (11), said power amplifier comprising: (a) a circuit means (3) for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier; (b) a detector circuit means (12) for detecting RF input to said amplifier and generating a driving signal (output signal from transistor 24) according to a power level of said RF input; (c) a self-adapting circuit means (27/28) for receiving said driving signal (the output signal from transistor 24 is part of the current mirror circuit formed by transistors 25/26) and

automatically modifying said bias signal and said quiescent current through said output transistor as mentioned in col. 5, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels as mentioned in col. 2, **meeting claim 7**.

Regarding claim 13, Matsumoto discloses in Fig. 6 a self-adapting circuit for dynamically controlling quiescent current flowing through said output transistor of a linear power amplifier operating in an output frequency band, having an output transistor (11), said linear power amplifier comprising a circuit means (3) for generating a bias signal producing a quiescent current flowing through said output transistor of said RF power amplifier, said self-adapting bias circuit comprising: a) a detector circuit means (12) for detecting RF input to said amplifier and generating a driving signal (output current from transistor 24) according to a power level of said RF input; b) means (27/28) for receiving said driving signal and automatically modifying said bias signal and said quiescent current through said output transistor as mentioned in col. 5, whereby said quiescent current at said output stage is reduced and optimized for minimum dissipation and optimal linearity at all power output levels as mentioned in col. 2, **meeting claim 13**.

Regarding claims 5, 11 and 17, Matsumoto further discloses the linear power amplifier as claimed in claims 1, 7 and 13, comprising first and second power output stages as shown in Fig. 1 or Fig. 2, wherein said detector circuit means (see Fig. 1, numeral 2) detects RF input to said amplifier at said first output stage (e.g. detail are shown in Fig. 2, numeral 01), for reducing said quiescent current at a second output stage (e.g. 02), since Matsumoto discloses e.g. in col. 2 "when the input power level is increased, the input current of the reference amplifier (detector

circuit means) is increased, so that the input currents supplied to **the respective stage amplifier** (note: the respective stage amplifier can be read as the "second stages" from the plurality of the unit amplifiers) are also increased", **meeting claims 5, 11 and 17**.

Allowable Subject Matter

Claims 3-4, 6, 9-10, 12, 15-16 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hieu Nguyen whose telephone number is 571-272-8577. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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hn

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